High-Aspect Ratio Deep Sub-Micron α-Si Gate Etch Process Control

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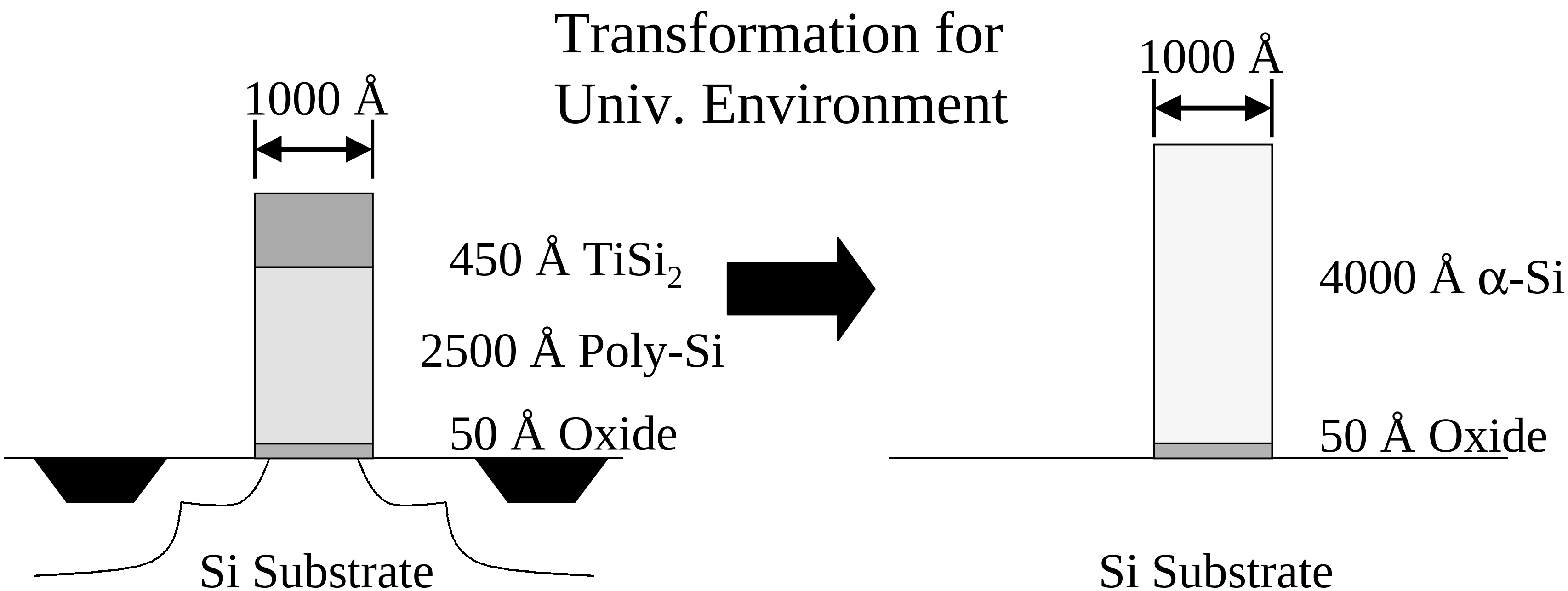
Overview of Talk

- Motivation and Project Goal
- Deep Sub-micron Etch Process Development: 0.1 μm Gate
- Real-Time Control of ME to OE Switch Point
- Application: Process Disturbance Rejection
    - Blank sample
    - Patterned sample
- Conclusion

Etching Process of Deep Sub-micron Structure

- **Problem sources**
  - Smaller feature size
  - Higher aspect ratio
  - Larger wafer size
- **Etching process problems**
  - Etch rate, and profile drift
  - Etch uniformity, and selectivity
  - Plasma damage, and contamination
- **Generic solutions**
  - Hardware development
  - Process development
  - Process control

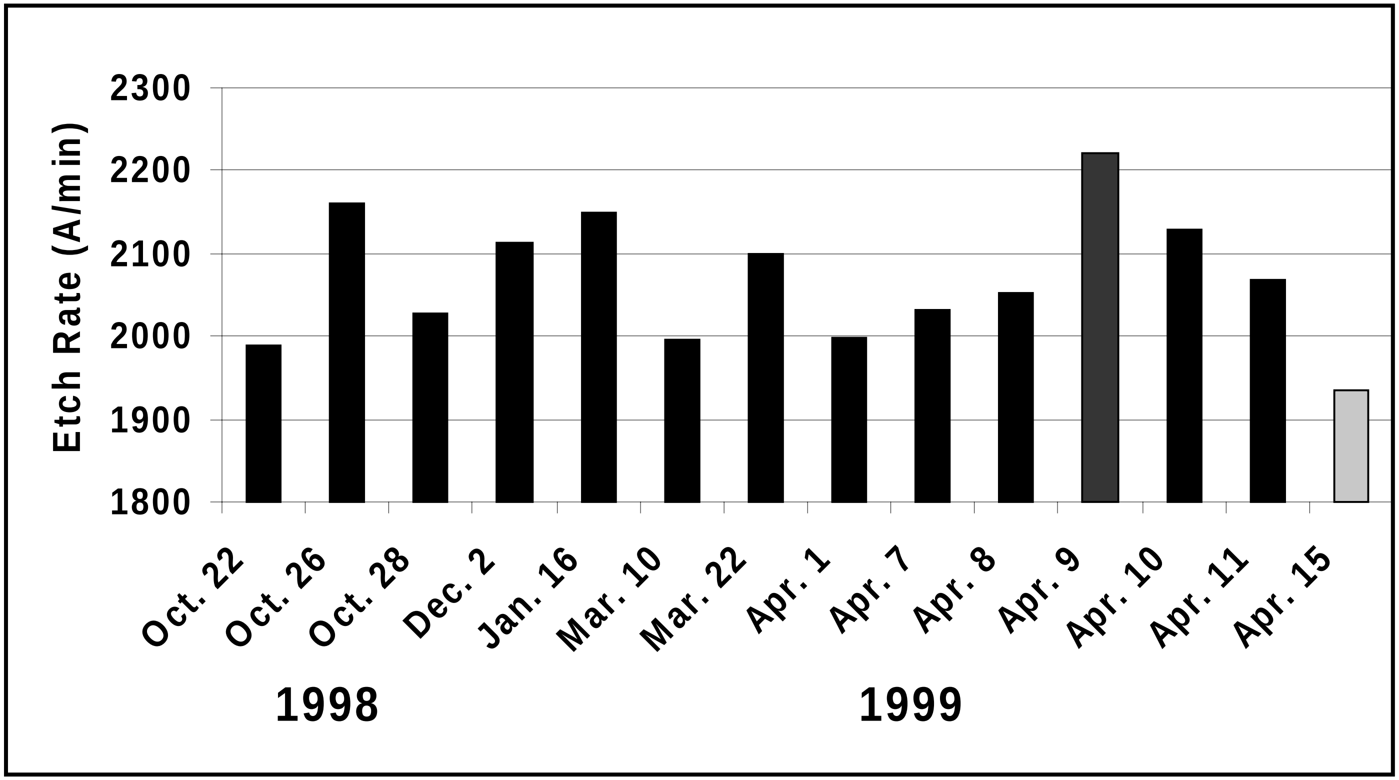
Vehicle for Process Control Investigation



Jorge et al. 1996, TI

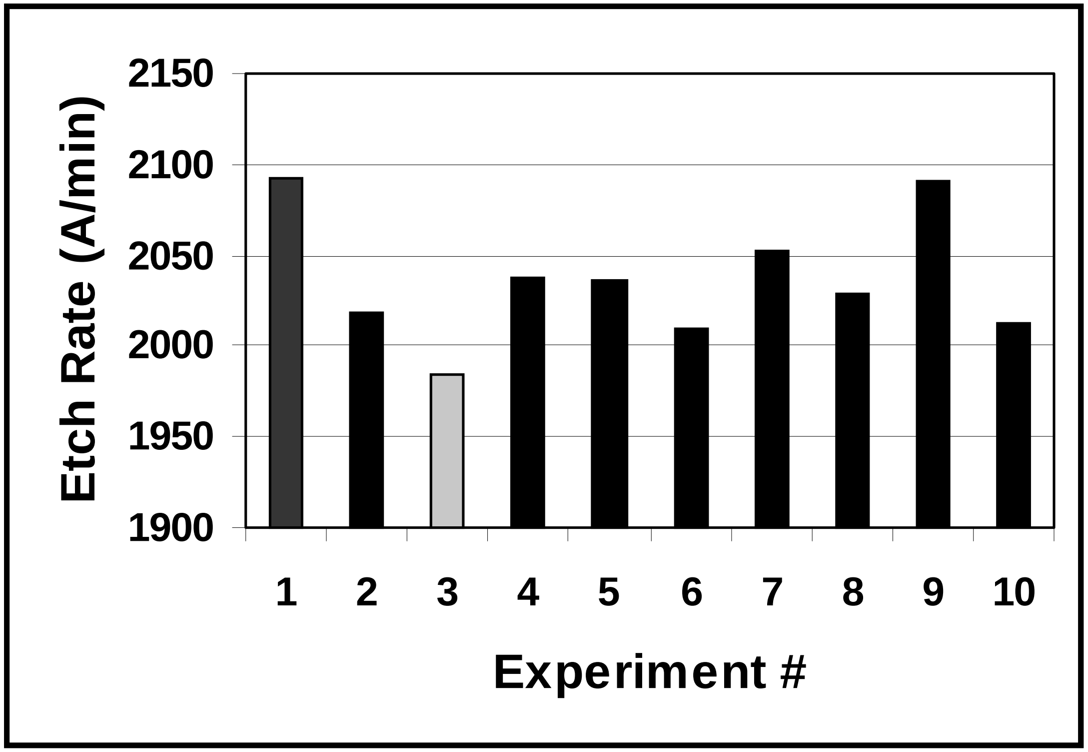
Our work

α-Si Etch Rate Drift: long term
(Lam TCP9400SE)



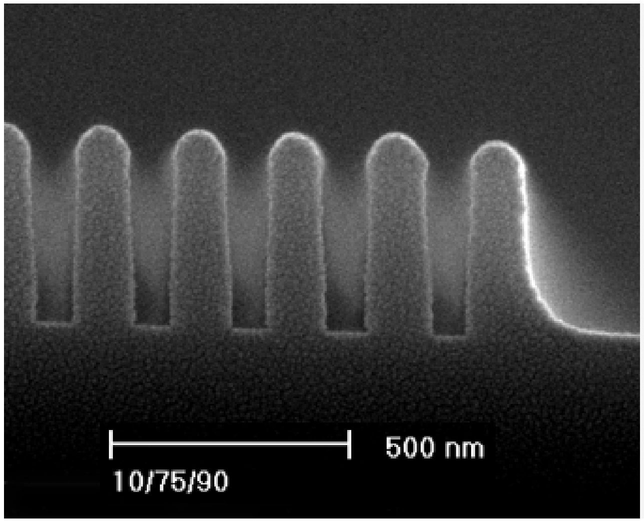
• Avg. etch rate: 2070 Å /min, 3 σ: 240 Å

Etch Rate Drift: short term (Mar. 13,1999)

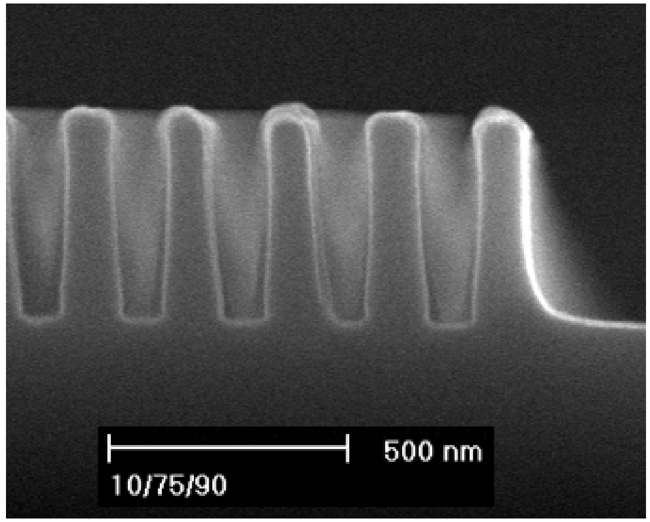


• Avg. etch rate: 2036 Å /min, 3 σ: 108 Å

Etch Profile Drift



July 16, 1998



July 27, 1998

0.1 μm oxide mask, 1:1 line-to-space ratio
4:1 aspect ratio
BT/ME/OE:10/75/90 seconds

Project Goal

- **Long-term Goal**

  Improve the repeatability of the etching process of 0.1 μm and below α-Si gate line

  - In situ morphology
  - Detection of real-time plasma variation via RF sensor

- **This Work**

  Improve etch profile repeatability through control of ME to OE switch point

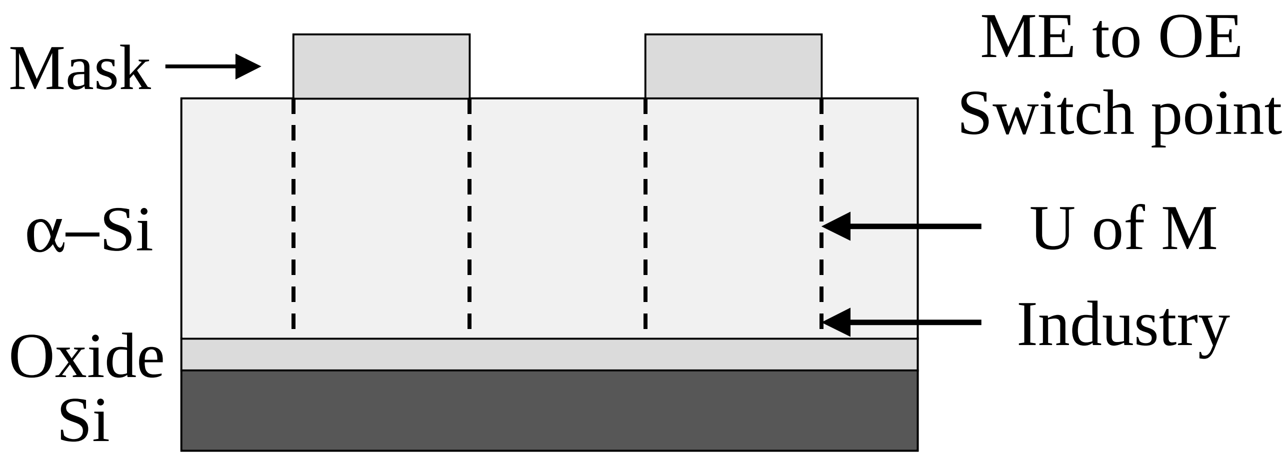
  - Real-time measurement and estimation of film thickness
  - Use of blanket test pad (S. W. Butler et al., 1994)
  - Real-Time Spectroscopic Ellipsometry (RTSE)

Process Development (I)

- **Oxide Mask Patterning Process**
  - E-Beam lithography
  - Lift-off process
  - 1:1, 1:3, and 1:10 line-to-space

- **Etching Process**
  - Three-step etching: BT, ME, and OE
  - Cl_2 and HBr plasma gas
  - Lam TCP9400SE plasma etching system

Process Development (II)



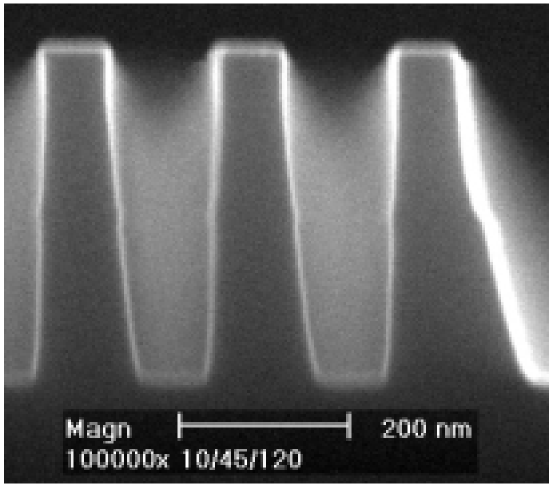
Industry Goal
- High throughput
- Good morphology
- Minimum gate oxide damage

Our Goal
- High throughput
- Thin mask oxide: must switch to OE before mask erosion

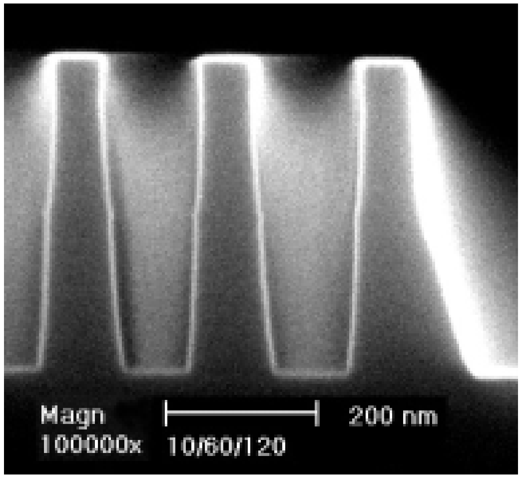
In neither case can we do the switch based on an OES signal

Importance of Proper Switch Point

(Etch Profiles: BT, ME and OE)



10/45/120 seconds



10/60/120 seconds

	Top	*Bottom*	*Space*
10/45/120	67	125	75
10/60/120	55	110	90 nm

Endpoint Detection

Motivation

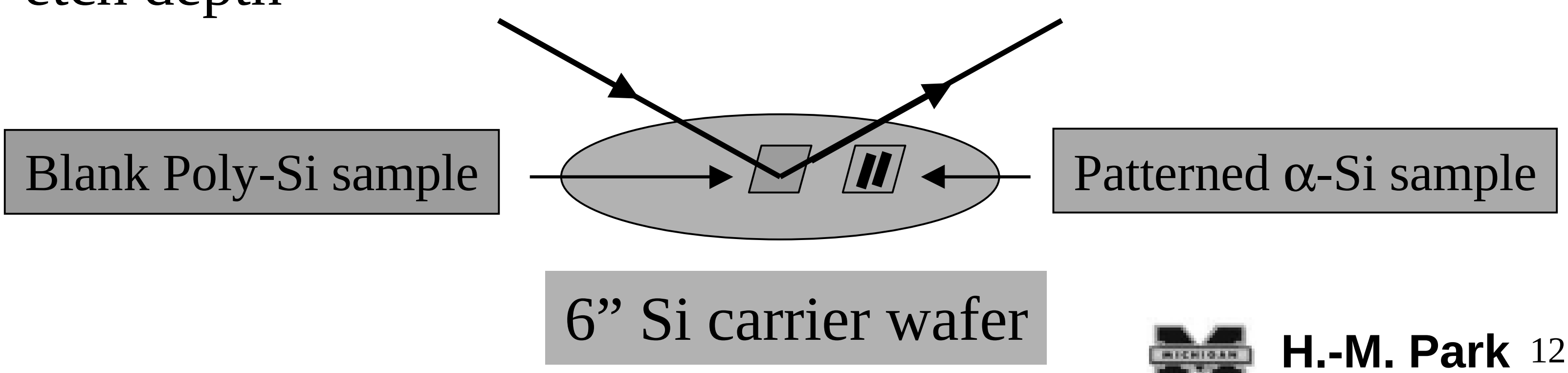
• Reduction of gate etch profile (CD) variation via accurate transition timing detection of ME to OE

Difficulty

• Cannot measure α-Si thickness via RTSE

Solution

• Estimate the α-Si etch depth via the measurement of n+ poly-si etch depth



Endpoint Detection (contd.)

Problem of n+ poly-si thickness measurement

• Slow measurement speed: 0.4 Hz (2.5 sec/measurement)

~ 10 nm change between measurements

• Time delay

- • Measurement delay: 0.18 sec
- • Thickness model fitting delay

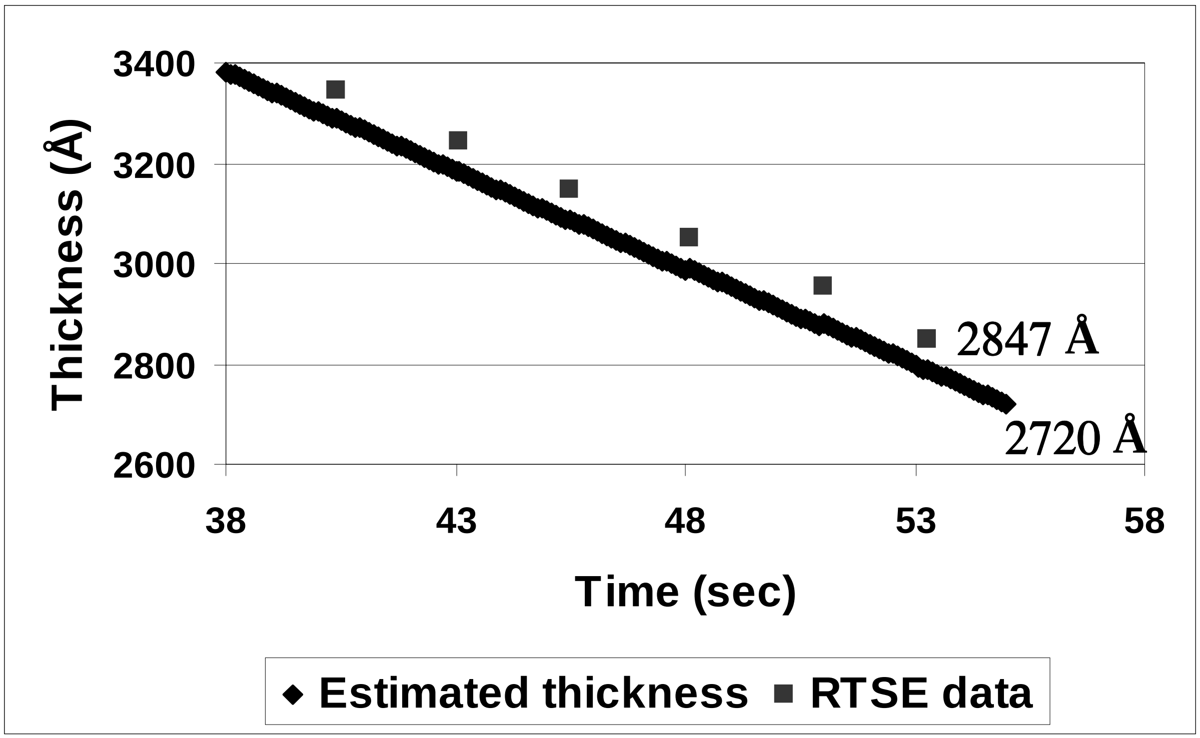
Solution

• Estimate the inter-measurements poly-si thickness with the use of a Kalman filter including the time delay

• Estimation interval: 0.1 sec

• 1 nm accuracy

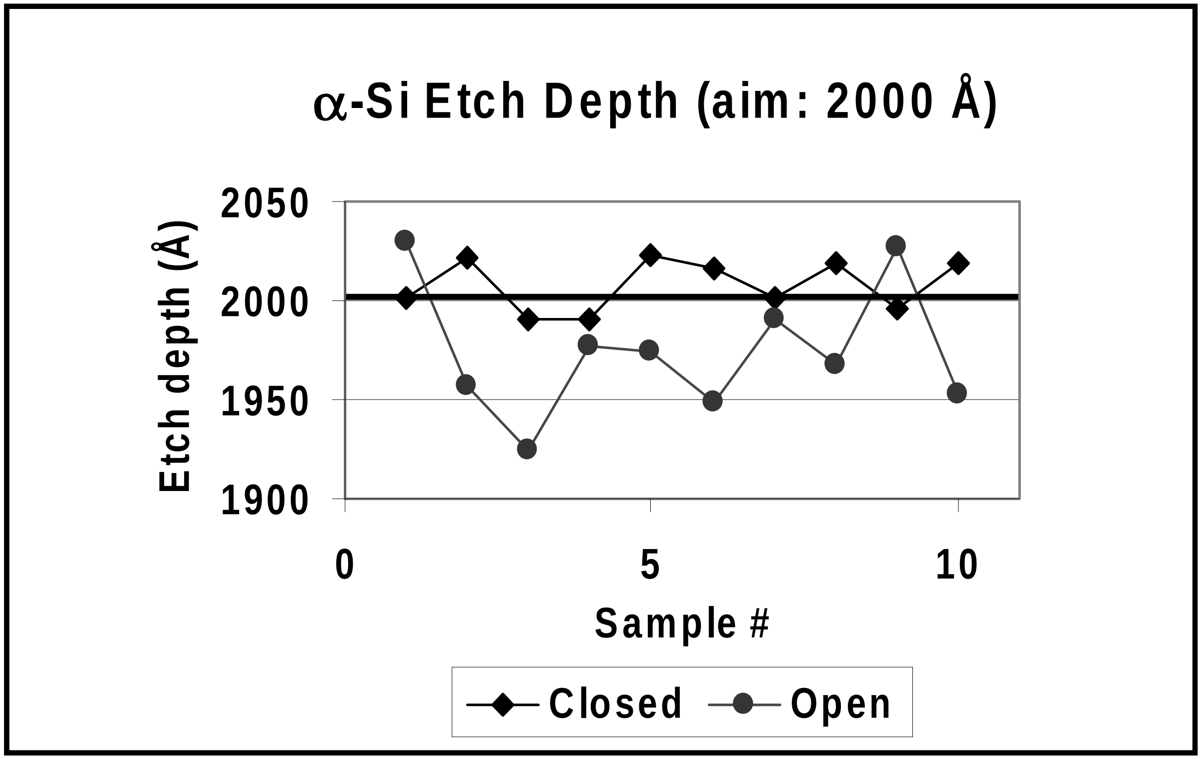
Endpoint Detection Experiment



- Detect n+ poly-si thickness within 1 nm error

α-Si Endpoint Detection Experiment

in Presence of Nominal Short-term Process Drift



Open loop: Avg:1975 Å
3 σ: 103

Closed loop: Avg: 2007 Å
3 σ : 39

Disturbance Rejection Experiment

Purpose

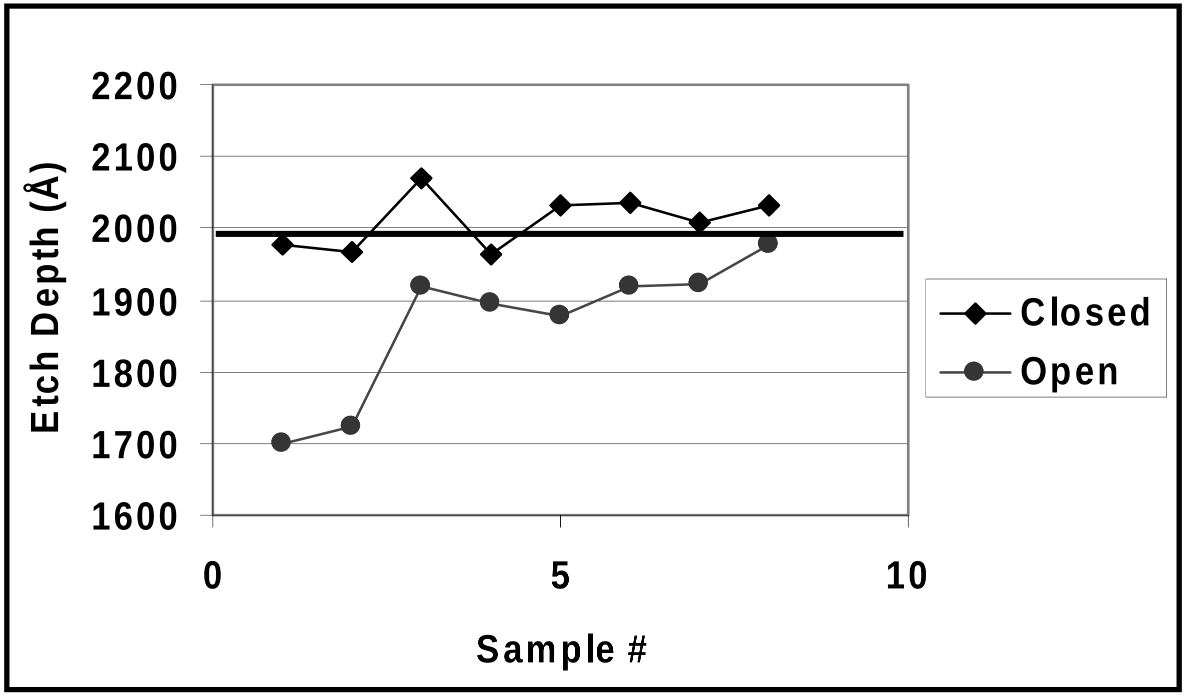
- To compare closed-loop endpoint detection to open-loop (timed-etch)

Method

- Intentional addition of disturbance
  - Chemical disturbance
    - Chamber wall condition: chamber venting
    - Cl_2 flow rate variation
  - Physical disturbance
    - Bias power variation

Disturbance Rejection

Chamber Venting

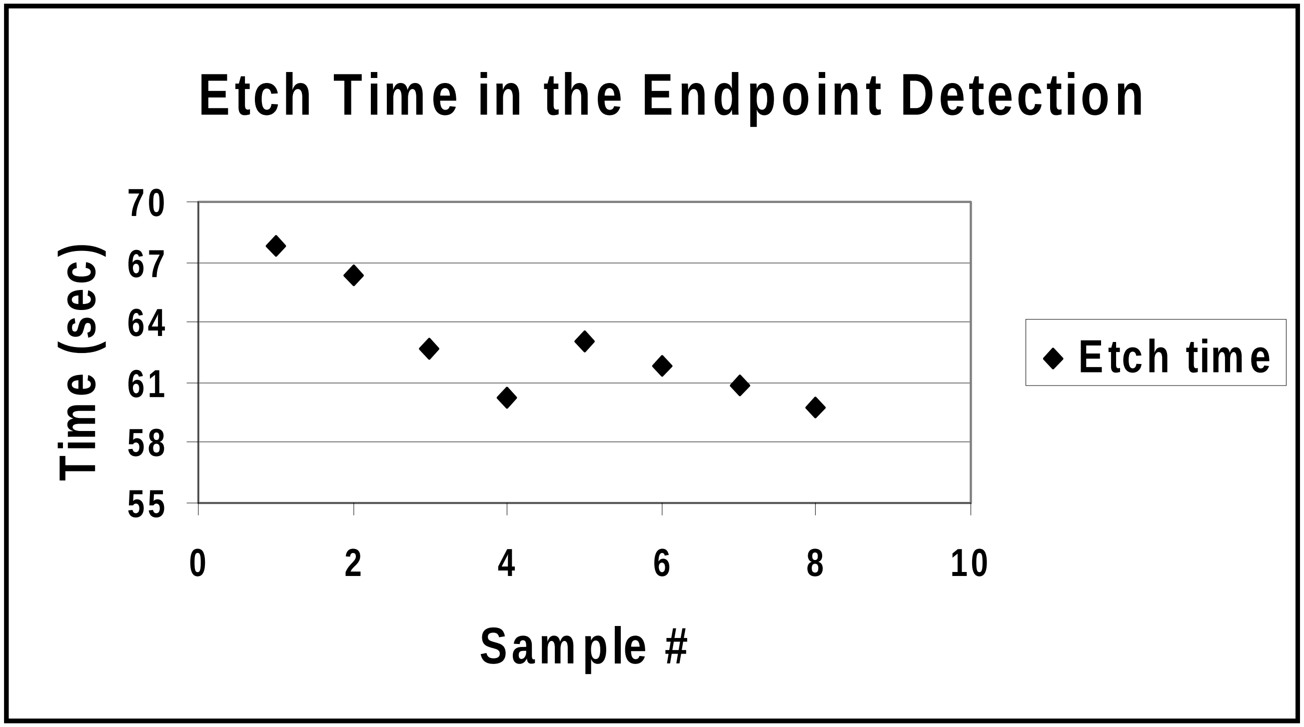


Open loop: Avg:1867 Å
3 σ: 303

Closed loop: Avg: 2011 Å
3 σ : 114

Disturbance Rejection

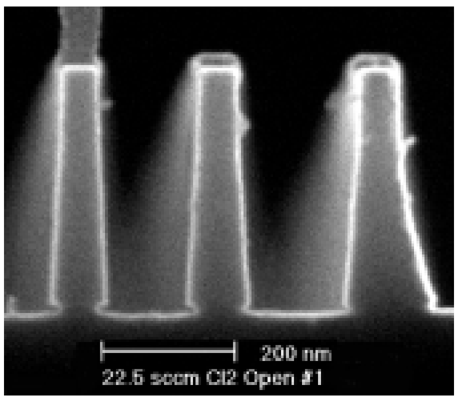
Chamber Venting



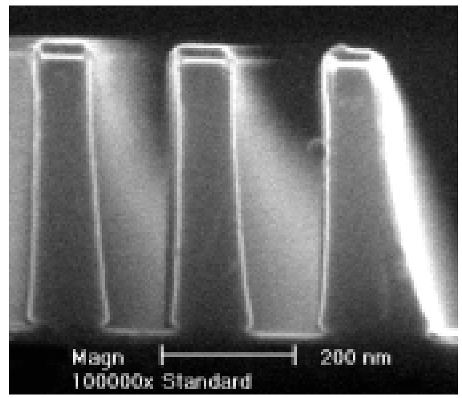
Open loop: 58.2 sec

Application to the Patterned Sample

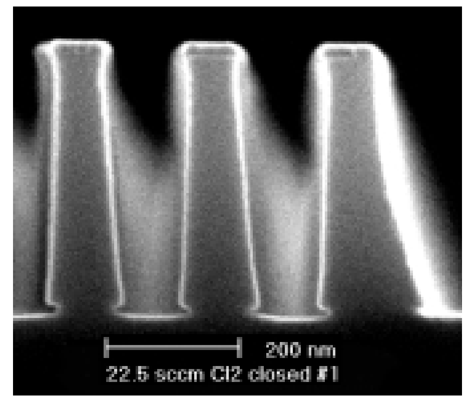
Cl_2 (+50%) Disturbance Rejection



Open loop: 60 sec ME



Standard etch
10/60/100 BT/ME/OE



Closed loop: 55.1 sec ME

	Top	*Bottom*	*Space*
Standard	72	113	87
Open	48	76	124
Closed	67	106	94 nm

Conclusion

- 0.1 μm and below, α-Si gate line mask patterning and etching processes were developed.
- The ME to OE transition timing is critical to the etch profile.
- Developed Automated α-Si ME endpoint detection algorithm
    - Real-time n+ poly-si thickness measurement
    - Kalman filter
    - 1 nm accuracy
- In limited experiments, automatic endpoint detection proves better performance than timed-etch with and without disturbance.